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**SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT**

Docket Number:
2885/10

Application Number
08/947,254

Filing Date
October 8, 1997

Examiner
G. RAY

Art Unit
2781

Invention Title
I/O AND MEMORY BUS SYSTEM FOR DFPs AND
UNITS WITH TWO- OR MULTI-DIMENSIONAL
PROGRAMMABLE CELL ARCHITECTURES

Inventor(s)
VORBACH et al.

Assistant Commissioner
for Patents
Washington D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

Date:

1/10/2001

Reg. No. P47893

Signature:

Andrew L. Reibman

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby bring the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.
2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed.

Dated:

1/10/01

By:

Andrew L. Reibman (Reg. No. P47893)

NOT CONSIDERED

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